WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of trench type device isolation regions formed in a semiconductor substrate;

a plurality of semiconductor active regions electrically isolated by the device isolation regions;

a first electrode layer self-aligned to the trench type device isolation regions; and

a second electrode layer formed over the first electrode layer with an insulating film interposed therebetween,

the top of each of the device isolation regions being located, in an area where the second electrode layer is present, at a first level below the top of the first electrode layer and above the surface of the semiconductor active regions and, in an area where the second electrode layer is not present, at a second level below the first level, and the surface of the semiconductor active regions being at substantially the same level in the area where the second electrode layer is present and in the area where the second electrode layer is not present.

2. The semiconductor device according to claim 1, wherein the semiconductor device is a nonvolatile semiconductor memory and, in the memory cell area in which memory cell transistors are formed, the first and second electrode layers constitute floating and control

gates, respectively, of each of the memory cell transistors.

3. The semiconductor device according to claim 2, wherein, in each of the memory cell area and the peripheral circuit area in which peripheral transistors are formed, the top of the device isolation regions in the area in which no second electrode layer is present is located at the second level.

4. The semiconductor device according to claim 3, wherein, in the peripheral circuit area, at least a portion of the first electrode layer is connected with the second electrode layer, and the first and second electrode layers form the gate electrode of each of the peripheral transistors.

5. A semiconductor device comprising:

a plurality of trench type device isolation regions formed in a semiconductor substrate;

a plurality of semiconductor active regions electrically isolated by the device isolation regions;

a first electrode layer self-aligned to the trench type device isolation regions; and

a second electrode layer formed over the first electrode layer with an insulating film interposed therebetween,

the top of each of the device isolation regions being located, in an area where the second electrode layer is present, at a first level below the top of

the first electrode layer and above the surface of the semiconductor active regions and, in an area where the second electrode layer is not present, at a second level below the first level, and the surface of the semiconductor active regions in the area where no second electrode layer is present being located at a level lower than in the area where the second electrode layer is present by the thickness of a thermal oxide film formed after the processing of the first electrode layer.

6. The semiconductor device according to claim 5, wherein the semiconductor device is a nonvolatile semiconductor memory and, in the memory cell area in which memory cell transistors are formed, the first and second electrode layers constitute floating and control gates, respectively, of each of the memory cell transistors.

7. The semiconductor device according to claim 6, wherein, in each of the memory cell area and the peripheral circuit area in which peripheral transistors are formed, the top of the device isolation regions in the area in which no second electrode layer is present is located at the second level.

8. The semiconductor device according to claim 7, wherein, in the peripheral circuit area, at least a portion of the first electrode layer is connected with the second electrode layer, and the first and second

electrode layers form the gate electrode of each of the peripheral transistors.

9. A nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

a plurality of trench type device isolation regions formed in a semiconductor substrate;

a plurality of semiconductor active regions electrically isolated by the device isolation regions;

a first layer of floating electrodes self-aligned to the trench type device isolation regions;

a second layer of floating electrodes formed on the first layer of floating electrodes to overlap with the device isolation regions; and

a layer of control electrodes formed over the second layer of floating gates with an interelectrode insulating film interposed therebetween,

the top of each of the device isolation regions being located, in an area where the control electrode layer is present, at a first level below the top of the second floating gate electrode layer and above the surface of the semiconductor active regions and, in an area where the control electrode layer is not present, at a second level below the first level, and the surface of the semiconductor active regions being located at substantially the same level in the area

where the control electrode layer is present and in the area where the control electrode layer is not present.

10. A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first electrode layer over the entire surface of the first insulating film;

selectively removing the first electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer;

etching the device isolation regions until the top of the device isolation regions in the memory cell area reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

forming a second insulating film over the entire surface of the semiconductor substrate;

removing a portion of the second insulating film over each of the peripheral transistors of the peripheral circuit area to form an opening that exposes a portion of the first electrode layer;

forming a second electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the second electrode layer;

patterning the second electrode layer using the gate masking pattern as a mask;

selectively etching away the second insulating film using the gate masking pattern as a mask;

etching the device isolation regions in the memory cell area until their top reaches the same level as the top of the first insulating film;

etching the device isolation regions in the peripheral circuit area until their top reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film; and

selectively etching away the first electrode layer using the gate masking pattern as a mask.

11. The method according to claim 10, wherein, in the memory cell area, the first and second electrode layers form the floating gate and the control gate, respectively, of each of the memory cell transistors, and, in the peripheral circuit area, the first and second electrode layers form the gate of each of the peripheral transistors.

12. A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral

circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first electrode layer over the entire surface of the first insulating film;

selectively removing the first electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer;

etching the device isolation regions until the top of the device isolation regions in the memory cell area reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

forming a second insulating film over the entire surface of the semiconductor substrate;

removing a portion of the second insulating film over each of the peripheral transistors of the peripheral circuit area to form an opening that exposes a portion of the underlying first electrode layer;

forming a second electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the second electrode layer;

patterning the second electrode layer using the

gate masking pattern as a mask so that its portion is left over the device isolation regions in the memory cell area;

selectively etching away the second insulating film using the gate masking pattern as a mask and the underlying patterned second electrode layer;

etching the device isolation regions in the peripheral circuit cell area until their top reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

etching the second electrode layer and the first electrode layer using the gate masking pattern as a mask under etching conditions of high selectivity to the second insulating film until the top of the first electrode layer reaches a level below the surface of the second insulating film in the memory cell area;

selectively etching away the second insulating film;

etching the device isolation regions until their top reaches the same level as the surface of the first insulating film; and

etching the first electrode layer using the gate masking pattern as a mask under etching conditions of high selectivity to the first insulating film to form stacked gates each of which is comprised of the first electrode of one-layer structure and the second electrode layer.

13. A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first floating gate electrode layer over the entire surface of the first insulating film;

selectively removing the first floating gate electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer, the top of the device isolation regions being at the same level as the surface of the first floating gate electrode layer;

forming a second floating gate electrode layer on the first floating gate electrode layer;

forming a control gate electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the control electrode layer;

patterning the control electrode layer using the gate masking pattern as a mask;

etching away the second insulating film using the gate masking pattern as a mask;

etching away the second floating gate electrode

layer using the gate masking pattern as a mask;

etching the first floating gate electrode layer until its top reaches a level midway between the top of the device isolation regions and the surface of the first insulating film;

etching the device isolation regions using the gate masking pattern as a mask until their top reaches the same level as the surface of the first insulating film; and

etching away the remainder of the first floating electrode layer using the gate masking pattern as a mask.